Reg. No. : ....

Name : ....

Sixth Semester B.Tech. Degree Examination, March 2015
(2008 Scheme)
08.605 : HIGH PERFORMANCE MICROPROCESSORS (R)
(Special Supplementary)

Time : 3 Hours　　　　　　　　　　　　　　　　　　　　　　　　Max. Marks : 100

PART – A

Answer **all**. **Each** question carries **4** marks.

1. Explain the following terms :

   Task privilege, descriptor privilege, selector privilege

2. How 80286 enter into protected mode ?

3. Explain the following signals :

   PEREQ, PEACK #, READY #, BUSY #

4. Discuss descriptor attribute bits in 80386.

5. Discuss out-of-order execution in Pentium-4.

6. Discuss the salient features of P4.

7. Explain instruction format in ARM.

8. What is the difference between the operation of a timer and counter in 8051 ?

9. What is the role played by timer 1 in serial communication ?

10. Discuss TCON register.

PART – B

Module – 1

11. Describe in detail about different registers of 80386.   **10**

12. Discuss cache mechanism in 80486.   **10**

OR

13. Explain the physical address formation in real addressing mode and protected virtual addressing mode in 80386.   **10**

14. Discuss the following techniques in Pentium processor.   **10**

    a) Trace cache

    b) Branch prediction

    c) Hyper threading technology.

Module – 2

15. Explain the addressing modes of ARM.   **10**

16. Describe the register-windowing techniques in SPARC.   **10**

OR

17. a) Explain the load-store architecture of ARM.   **5**

    b) Explain the conditional execution property of ARM.   **5**

    c) Explain the circular buffer organization of registers in RISC.   **10**

Module – 3

18. With a frequency of 22 MHz, generate a frequency of 100 KHz on Pin 2.3 of 8051. Use Timer-1 in mode 1.   **10**

19. Take data in through ports 0,1 and 2 one after the other and transfer this data serially, continuously.   **10**

OR

20. Discuss the architecture of 8051 with a neat block diagram.   **10**

21. Assuming that XTAL = 22 MHz, write a program to generate a square wave of frequency 1 KHz on Pin 1.2.   **10**